CLAIMS:

1. An RF transponder (102, 200, 400) comprising a plurality of circuits (200, 400), and a power supply (222, 422, 423) for providing power (Vxx, Vcc, Vdd), including an input voltage (Vxx), to the plurality of circuits, the RF transponder characterized in that:

a one of the plurality of circuits comprises a Power-On Reset (POR) circuit (482, 600) for generating a reset signal (INT_RES, RESET) for maintaining other ones of the plurality of circuits in an inoperative reset mode unless the power supply has sufficient power (Vstart, Vsustain) to ensure proper operation of the other ones of the circuits; and

at least one of the other ones of the plurality of circuits comprises control logic (440, 442) which, upon release of the reset signal, starts transmission of a data stream at a first bit of the data stream, in order to ensure a first-pass transmission of a complete data stream.

2. An RF transponder, according to claim 1, characterized by:

a flip-flop circuit (650) for setting and clearing a state of the reset signal; and

an init delay circuit (620), connected to an input of a comparator (634), for controlling the flip-flop circuit so that the flip-flop circuit holds the reset signal in an ON-state for a delay time (Ramp_Delay) after abrupt power-up of the transponder.

3. An RF transponder, according to claim 1, characterized by:

a flip-flop circuit (650) for setting and clearing a state of the reset signal; and

a voltage divider (610) connected to a first comparator (638), for providing an input signal (V_SUSTAIN) to a voltage limit circuit (640); wherein the voltage limit circuit controls the flip-flop circuit so that the flip-flop circuit sets the reset signal in response to the input voltage being less than or equal to a minimum sustaining voltage (Vsustain), and clears the reset signal in response to the input voltage being greater than the minimum sustaining voltage.

4. An RF transponder, according to claim 3, characterized in that:

the minimum sustaining voltage has different values (Vsustain(active), Vsustain(passive), Vstart) in different transponder operating modes (active, passive).

5. An RF transponder, according to claim 4, characterized in that:

in an active transponder operating mode, the power supply derives power for the plurality of circuits from a battery; and

in a passive transponder operating mode, the power supply derives power for

the plurality of circuits from an RF signal received by an antenna system (210, 410).

6. An RF transponder, according to claim 3, characterized by:

a second comparator (636) connected to the voltage divider and providing an input signal (V_START) to the voltage limit circuit; wherein the voltage limit circuit controls the flip-flop circuit so that the flip-flop circuit sets the reset signal while the input voltage is increasing from less than or equal to a minimum sustaining voltage (Vsustain) to a minimum starting voltage (Vstart), and clears the reset signal when the input voltage increases above the minimum starting voltage.

7. An RF transponder, according to claim 6, characterized by:

logic (633f, 642, 644, 646, 648, 633e) in the voltage limit circuit for combining the input signal from the first comparator and the input signal from the second comparator so that, after the input voltage has increased above the minimum starting voltage, the flip-flop circuit maintains a cleared reset signal state as long as the input voltage remains above the minimum sustaining voltage, and so that after the input voltage has increased above the minimum starting voltage, the flip-flop circuit sets the reset signal when the input voltage decreases to less than or equal to the minimum sustaining voltage.

8. An RF transponder, according to claim 3, characterized by:

an init delay circuit (620) connected to an input of a second comparator (634) which shares control of the flip-flop circuit with the voltage limit circuit, so that the flip-flop circuit holds the reset signal in an ON-state after the beginning of power-up for a longer one of a first period of time which is a delay time (Ramp_Delay) and a second period of time which is a time expended while the input voltage increases to greater than a minimum voltage (Vsustain, Vstart).

9. An RF transponder, according to claim 1, characterized by:

an input (RES) for an external reset signal (EXT_RES); and

at least one logic element (658, 633c), for combining the external reset signal with the POR-generated reset signal (INT_RES) and forming a combined reset signal (RESET), wherein the combined reset signal is set in response to either the external reset signal or the POR-generated reset signal being set, and the combined reset signal is cleared when the external reset signal and the POR-generated reset signal are both clear.

10. An RF transponder, according to claim 9, characterized by:

a gate (N30) connected between ground and the input for the external reset

signal, wherein the gate is controlled by a one (Vdd) of the power supply voltages so that the external reset signal is cleared when the power supply voltage is at a level suitable for logic control.

11. An RF transponder, according to claim 1, characterized in that:

the power for the POR circuitry is the highest available regulated voltage (Vxx); and

components of the Power-On Reset circuit are selected for minimal power use and for operation at the lowest possible voltages, so that the Power-On Reset circuit is functional before the other ones of the plurality of circuits.

12. An RF transponder, according to claim 11, characterized in that the Power-On Reset circuit comprises:

low current, three-stage comparators (634, 636, 638);

Schmitt trigger inverters (631b, 631c, 631d); and

a low current voltage divider (610), utilizing on-chip, high value poly resistances.

13. Method of controlling operation of an RF transponder (102, 200, 400) during power-up and power-down, wherein the RF transponder comprises a plurality of circuits (200, 400) and a power supply (222, 422, 423) for providing power (Vxx, Vcc, Vdd), including an input voltage (Vxx), to the plurality of circuits, the method characterized by:

generating a reset signal (INT_RES, RESET) for maintaining selected ones of the plurality of circuits in an inoperative reset mode unless the power supply has sufficient power (Vstart, Vsustain) to ensure proper operation of the plurality of circuits; and

upon release of the reset signal, starting data transmission with a first bit of a data stream to be transmitted, in order to ensure a first-pass transmission of a complete data stream.

14. Method, according to claim 13, characterized by:

holding the reset signal on for a delay time (Ramp_Delay) after abrupt power-up of the transponder.

15. Method, according to claim 13, characterized by:

setting the reset signal in response to the input voltage being less than or equal to a minimum sustaining voltage (Vsustain), and

clearing the reset signal in response to the input voltage being greater than the minimum sustaining voltage.

16. Method, according to claim 15, characterized by:

selecting a value for the minimum sustaining voltage to different values (Vsustain(active), Vsustain(passive), Vstart) for transponder operation based on different operating modes (active, passive) for the RF transponder.

17. Method, according to claim 16, characterized in that:

in an active transponder operating mode, the power supply derives power for the plurality of circuits from a battery; and

in a passive transponder operating mode, the power supply derives power for the plurality of circuits from an RF signal received by an antenna system (210, 410).

18. Method, according to claim 15, characterized by:

setting the reset signal while the input voltage is increasing from less than or equal to a minimum sustaining voltage (Vsustain) to a minimum starting voltage (Vstart), and

clearing the reset signal when the input voltage has increased above the minimum starting voltage.

19. Method, according to claim 18, characterized by:

clearing the reset signal after the input voltage has increased above the minimum starting voltage,

maintaining the cleared state of the reset signal while the input voltage remains above the minimum sustaining voltage; and

after the input voltage increases above the minimum starting voltage, setting the reset signal when the input voltage decreases to less than or equal to the minimum sustaining voltage, then maintaining the set state of the reset signal while the input voltage remains below the minimum starting voltage.

20. Method, according to claim 15, characterized by:

holding the reset signal in an ON-state after the beginning of power-up for a longer one of a first period of time which is a delay time (Ramp_Delay) and a second period of time which is a time expended while the input voltage increases to greater than a minimum voltage (Vsustain, Vstart).

21. Method, according to claim 13, characterized by:

setting a combined reset signal (RESET) when either an externally-supplied reset signal (EXT_RES) or the transponder-generated reset signal (INT_RES) is set; and

clearing the combined reset signal when both the external and the transponder-generated reset signals are clear.

22. Method, according to claim 21, characterized by:

clearing the externally-supplied reset signal whenever the voltage level of the power supply is suitable for digital logic control.

23. Method, according to claim 13, characterized in that:

the power for the transponder circuitry generating and releasing the reset signal is the highest available regulated voltage (Vxx); and

causing transponder circuitry which generates and releases the reset signal to be functional before the other ones of the plurality of circuits become functional.